Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1. (Currently Amended) A method including:

detecting a power management event in a system that includes a change in a system power between an external power source and a battery source;

and

~~dynamically adjusting,~~ in response to the power management event, a system management controller multiplexes multiple management commands onto a system management bus in one signal for transmission to multiple system components to change settings of performance registers inside the system components, including dynamically adjusting a frequency of a processor clock, a memory subsystem clock, a clock generator, adjust a voltage supplied to the multiple system components, and ~~a voltage level and clock frequency level provided to a plurality of system components including a microprocessor and system buses, including~~ adjust~~ing~~ a chipset buffer strengt~~h~~.

2. (Canceled).

3. (Previously Presented) The method of claim 1, wherein a system chipset drives the system buses.

4. (Previously Presented)

5. (Previously Presented) The method of claim 1, wherein the components include a memory subsystem and a graphics subsystem.

6. (Previously Presented) The method of claim 1, wherein the dynamically adjusting includes adjusting performance states of the plurality of system components between a high level and a low level.

7. (Canceled).

8. (Previously Presented) The method of claim 1, wherein adjusting the performance state of a graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

9. (Previously Presented) The method of claim 6 , wherein dynamically adjusting the performance states includes automatically placing the system in a deep sleep state upon the occurrence of the power management event to adjust the performance states of the system components.

10-18. (Canceled)

19. (Currently Amended) A system comprising:

a detector adapted to detect generation of a power management event that includes a change in a system power between an external power source and a battery source; and

a controller ~~to automatically adjust~~, in response to the power management event, to multiplex multiple management commands onto a system management bus in one signal for transmission to multiple system components to change settings of performance registers inside the system components, including to dynamically adjust a frequency of a processor clock, a memory subsystem clock, a clock generator, adjust a voltage supplied to the multiple system components, and adjust a chipset buffer strength.

~~voltage level and clock frequency level provided to a plurality of system components including a microprocessor and system buses, and to adjust a chipset buffer strenght~~.

20. (Canceled).

21. (Previously Presented) The system of claim 19, wherein a system chipset drives the system buses.

22. (Previously Presented)

23. (Previously Presented) The system of claim 19, wherein the components include a memory subsystem and a graphics subsystem.

24. (Previously Presented) The system of claim 19, wherein the dynamically adjusting includes adjusting performance states of the plurality of system components between a high level and a low level.

25. (Canceled).

26. (Previously Presented) The system of claim 24, wherein adjusting the performance state of a graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics

performance levels.

27. (Previously Presented) The system of claim 24, wherein the low level is a deep sleep state.

28. (Previously Presented)

29. (Canceled).

30. (Canceled)

31. (Canceled)

32. (Canceled)

33. (Canceled)

34. (Canceled).

35. (Canceled)

36. (Canceled)

37. (Currently Amended) A computer-readable medium having stored thereon a set of instructions to translate instructions, the set instructions, which when executed by a processor, cause the processor to perform a method comprising:

detecting a power management event that includes a change in a system power between an external power source and a battery source; and

in response to detecting the power management event, a system management controller multiplexing multiple management commands onto a system

management bus in one signal for transmission to multiple system components to change settings of performance registers inside the system components, including to dynamically adjust a frequency of a processor clock, a memory subsystem clock, a clock generator, adjust a voltage supplied to the multiple system components, and adjust a chipset buffer strength.

~~dynamically adjusting, in response to the power management event, a voltage level and clock frequency level provided to a plurality of system components including a microprocessor and system buses, including adjusting a chipset buffer strenght.~~.

38. (Canceled).

39. (Previously Presented) The computer-readable medium of claim 37, wherein a chipset drives the system buses.

40. (Canceled) ~~The computer-readable medium of claim 37, further includes adjusting a chipset buffer strength.~~

41. (Previously Presented) The computer-readable medium of claim 37, wherein the components Currently Amended a memory subsystem and a graphics subsystem.

42. (Previously Presented) The computer-readable medium of claim 41, wherein the dynamically adjusting includes adjusting performance states of the plurality of system components between a high level and a low level.

43. (Canceled)

44. (Previously Presented) The computer-readable medium of claim 42,

wherein adjusting the performance state of a graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

45. (Previously Presented) The computer-readable medium of claim 42, wherein dynamically adjusting the performance states includes automatically placing the system in a deep sleep state upon the occurrence of the power management event to adjust the performance states of the system components.